LABORATÓRIO ABERTO DE FÍSICA NUCLEAR

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Proposal	N° 122 (cont)
Title: **Irradiation of electronic devices**	
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Spokeperson: **Nemitala Added**	e-mail: **nemitala@if.usp.br**
Telephone: 3091-6824	Skype:
Number of days for experiment:	40 days
Period planned for the experiment (are the setup ready for beam time?): Experiment can be performed tomorrow	

Technical information

Ion source			Accelerator			Experimental Area	
Beam	Cathode	$I_{mínima}$	V_{min}	V_{max}	Bunched beam?	Beam line	Target
Several		200 nA	6,5	8,0	n	0	several

Other relevant/needed information:

Cathode with mixture of elements (C, O, F, Si, Cl, Ti, Cu, Ag)

3-4 days each month

Irradiation of eletronic devices

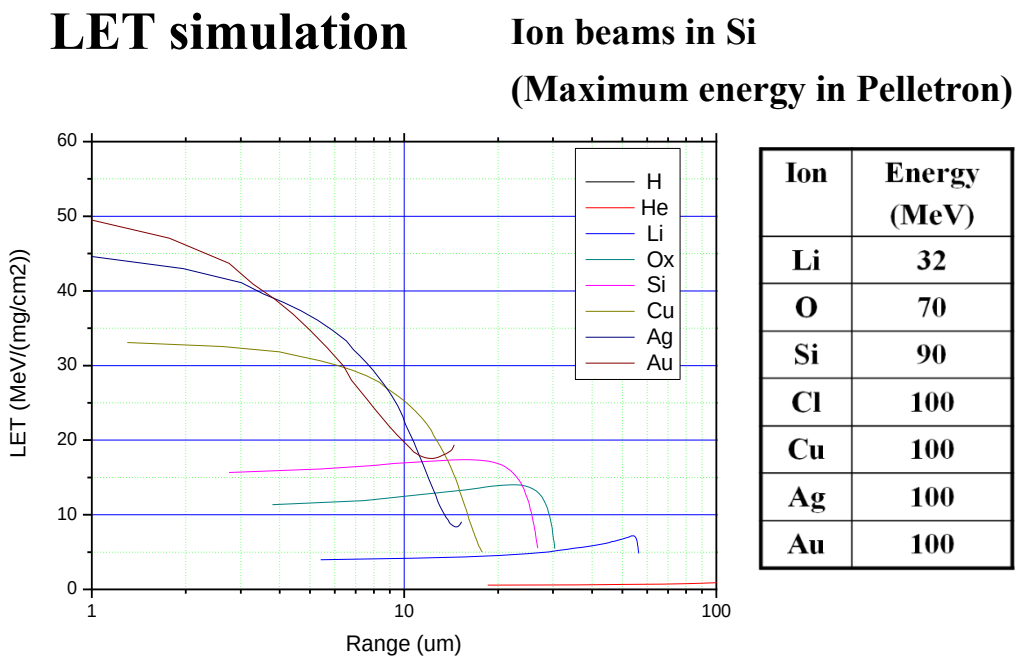
The study of ionizing radiation effects on materials used in electronic devices is of great relevance for the progress of global technological development and, particularly, it is a necessity in some strategic areas in Brazil like the construction of satellites [1]. Electronic circuits are strongly influenced by radiation and the need for IC´s featuring radiation hardness is largely growing to meet the stringent environment in space electronics. On the other hand, aerospace agencies are encouraging both scientific community and semiconductors industry to develop hardened-by-design components using standard manufacturing processes to achieve maximum performance, while significantly reducing costs. To understand the physical phenomena responsible for changes in devices exposed to ionizing radiation several kinds of radiation should then be considered, among them heavy ions, alpha particles, protons, gamma and X-rays. Radiation effects on the integrated circuits are usually divided into two categories: Total Ionizing Dose (TID), a cumulative dose that shifts the threshold voltage and increases transistor's off-state current; Single Events Effects (SEE), a transient effect which can deposit charge directly into the device and disturb the properties of electronic circuits [2]. TID is one of the most common effects and may generate degradation in some parameters of the CMOS electronic devices, such as the threshold voltage oscillation, increase of the sub-threshold slope and increase of the off-state current. The effects of ionizing radiation are the creation of electron-hole pairs in the oxide layer changing operation mode parameters of the electronic device. Indirectly, there will be also changes in the device due to the formation of secondary electrons from the interaction of electromagnetic radiation with the material since the charge carriers can be trapped both in the oxide layer and in the interface with the oxide. In this work we will investigate the behavior of MOSFET devices fabricated with different geometries, using heavy ion and proton beams.

First tests were done using the 1.7 MV 5SDH tandem Pelletron accelerator of the USP Physics Institute with a proton beam of 2.6 MeV. Nevertheless, it is necessary to use heavy ion beams such as ^{28}Si, ^{37}Cl and ^{107,109}Ag in the energies produced by the Tandem 8MV Pelletron accelerator and the new Linear Accelerator (under construction) to achieve the high values of Linear Energy Transfer specified in standards used to characterize the electronic devices. A new beam line (0 degree) was installed in the Pelletron experimental hall aiming the irradiation of different samples. The characteristics of the new setup were planned to attend the requirements of European Space Agency (ESA) for irradiation of electronic devices: large area with an homogeneous beam, flux ranging from 10^2 to 10^7 p/s/cm^2. Another feature of the new setup is a 4D goniometer controlling the target holder, allowing changes in the irradiation area or in the angle of incidence of beam.

This new setup allowed to perform Single Event Effects (SEE) in the electronic devices varying the LET and intensity of beam using different projectiles like ^{10}B, ^{12}C, ^{16}O, ^{28}Si, ^{35}Cl, ^{107}Ag. Several collaborations with other groups were stablished in order to calculate the cross sections for the SEE for different devices and technologies as well as to evaluate mitigation procedures to prevent misinformation related to charge deposit in the devices.

We like to point out our participation in the CITAR project (Desenvolvimento de circuitos integráveis tolerantes a radiação) supported by Finep and MCTI. Several institutions were involved (INPE, FACTI, AEB, IEAv, IF, FEI, IMT) in the project that aimed to build new devices and setups to be used in the Brazilian sattelites. INPE and FACTI were responsible

for the management of project. The measurements performed by our group were fundamental to evaluate the progress in the development of new devices and mitigation processes in this project.



Ion	Energy (MeV)
Li	32
O	70
Si	90
Cl	100
Cu	100
Ag	100
Au	100

Figure 1: LET simulation (TRIM code) for projectiles using typical conditions in Pelletron accelerator.

[1] Duzellier, S., "Radiation Effects on Electronic Devices in Space", Aerospace Science and Technology 9, pag. 93-99, 2005.
[2] Barnaby, H.J., "Total-Ionization-Dose Effects in Modern CMOS Technologies", IEEE Transactions on Nuclear Science, vol. 53, n° 6, 2006.

Relação de alguns dos experimentos planejados para o próximo período:

Teste de SEUs em SoC e FPGA

Fábio Benevenuti e Fernanda L Kastensmidt (UFRGS)

Irradiation tests with heavy ions on programmable devices including systems on chip (SoC) and programmable logic (FPGA), for evaluation of single-event effects (SEE, single-event upset) on storage elements (SEU, single-event upset).
The experiment includes the investigation of mitigation techniques, both software-based (SIHFT) and hard-based (e.g. TMR), and the qualification of software and hardware designs, including hard-core microprocessors present in the SoC (Arm Cortex-M and Cortex-A) and soft-core microprocessors implemented in the FPGA (Arm Cortex-M and RISC-V), as well as dedicated hardware accelerators for machine learning processing (e.g. AMD Xilinx DPU).

Target devices include SoC Infineon/Cypress PSoC5LP, manufactured in 130 nm technology, SoC+FPGA AMD Xilinx APSoC Zynq-7000, manufactured in 28 nm technology, and FPGA NanoXplore NX1, manufactured in 65 nm RHBD/SPACE technology.
The beams typically used for the experiments are ^{16}O with energies on the surface of the device in the order of 35 to 50 MeV (SoC PSoC5LP and APSoC Zynq-7000), ^{12}C with energy in the order of 40 MeV (APSoC Zynq-7000) , and ^{28}Si with energy around 65 MeV (FPGA NX1). The flux typically used in the experiments is in the order of 2×10^{2} $cm^{-2}.s^{-1}$ to 6×10^{3}, depending on the target device (SoC or FPGA) and manufacturing technology.
Considering the diversity of devices and software and hardware configurations to be investigated, it is requested to allocate 3 periods of irradiation per year, of 5 working days each, which also include the time required for setting up the experiment, focusing the beam and calibration.

Irradiation of MicroSemi ProAsic3 + spacewire communicaton protocol

Saulo Finco (CITAR Collaboration)

CTI's "Hardware Systems Design Center" has been working in the field of microelectronics for many years with the development of various chips. With the start of the CITAR project, in addition to the development of ASICs, there is also an interest in testing these chips in conditions that "simulate the space environment". One of the necessities is to perform tests of the type SEE (Single Event Effects), that are the effects caused in the electronics by a single particle (as opposed to the effect accumulated in years of operation in the space). The importance of Pelletron to the CITAR project is so significant that the CITAR project contributed (including financially) with IFUSP / Pelletron to have new beam lines built and installed to improve their suitability for SEE type tests on electronic components. institutions (federal, state and private), IFUSP is one of the co-executors of the CITAR project.
There is interest in the CITAR project in studying these various SEE effects in a number of electronic components. To exemplify some, here is a list that is not complete
* Latch-up (SEL) caused by ions on any type of electronic components. Latch-ups are serious events and there are 2 types:
  - Destructive - the chip is lost
  - Non-destructive - it is necessary to switch the component off and on again to restore normal operation.
* Transients (SET) in "important signals" that cause a malfunction on the chip.
  - In the case of digital chips, the extremely critical lines are the RESET and CLOCK and writing signals in asynchronous memories.
  - But in addition, we also have varied glitches, LVDS signals, PLL operation, increase in noise level in A / D converters and others.
* Upsets (SEU) or bit-flips on memory elements
  - Bit-flips in unprotected registers (occurs in lower power)
  - Bit-flips on protected registers (high power needs)
  - Bit-flips on non-protected SRAM memories
  - Bit-flips in protected SRAM memories (error correction codes, voters, redundancies...)
  - Bit-flips in non-protected FLASH memories

* Single Event Functional Interrupts (SEFI) - which occurs when the control of a processor and / or state machine is "corrupted" by placing the circuit in an undefined state, or test mode, or stopped. A reset or power cycle may be required to restore the normal operating condition
  - study of SEFI in FSM (state machines)
  - SEFI study on processors

Future tests

* ASIC TeleComando
* ASIC SpaceWire

- SpaceWire communication between 2 devices with error rate measurement (BER) and other types of protocol errors
- Constant monitoring of the voltages 1V8, 3V3 and the temperature of the chip
- Run other samples of ASICs at low voltages (1.65V).
- Survey of the LETth curve of some structures
- Specific tests to monitor PLL

* ASIC Power Key

Comparing Rectangular and ELT MOSFET layouts under TID

M.A. Guazzelli - Centro Universitário FEI (coord)

ELT (Enclosed Layout Transistor) is a different layout of a MOS transistor in terms of shape. The ELT MOSFET transistor works the same way as the conventional MOS transistor, the difference is in the manufacturing layout. The ELT (Enclosed Layout Transistor) promotes better isolation in one of the source or drain terminals because are completely surrounded by a layer of polysilicon. The group of designers from CTI (Center for Information Technology) provided two integrated circuits (P-MOS Power Transistors, PPT), each with five P-MOSFET devices in 0.6 µm SOI-CMOS technology, three of them with layout rectangular and the other two with ELT layout structures. This study aims to compare the behavior of rectangular devices and ELTs (Common Emitter Logic Transistors) subjected to the same conditions of exposure to the effects of ionizing radiation. We propose the use of SAFIIRA located in the zero degree pipeline of the 8 MV Pelletron accelerator at the Open Laboratory of Nuclear Physics (LAFN) of the USP Institute of Physics to carry out the study of the effects caused by heavy ions. In this laboratory, beams of different ions (^{16}O, ^{19}F, ^{28}Si, ^{35}Cl, ^{65}Cu) will be accelerated with voltages varying between 6 and 8 MeV. The objective is to investigate the sensitivity curve of the cross section of the device in relation to the transfer of energy from the ions to the material. Measurements will be performed simultaneously on different devices, both rectangular and ELT formats, allowing a direct comparison of their tolerance to Electronic Special Effects (SEE).

A period of 7 days of machine time will be required to assemble and test the necessary instrumentation.

Sensores CMOS

Renato Giacomini – Depto Engenharia Elétrica – FEI (coordinator)

CMOS sensors are composed of light-sensitive elements that, depending on the intensity of light incident on them, generate an electrical signal or electrical charge. These sensors offer advantages such as low power consumption, lower cost compared to CCDs, random access image data, selective readout mechanisms, and high imaging speed. Many of these sensors are used as image capture devices in environments particularly subject to radiation, such as hospitals and outdoor environments. It is essential to characterize such devices, to estimate the generation of noise, errors in images and deterioration due to ageing.

In this proposal, we will study the gated PIN side photodiode manufactured using GF BiCMOS 8HP 0.13 technology, an IBM commercial manufacturing process provided by the MOSIS university support program. In the planned experiment at the Pelletron, the objective is to study the destructive and non-destructive effects of the incidence of ions from different LETs. In the experiment, we intend to explore the current pulses generated by Single Event Effects (SEE) with the device under polarization and without polarization. In addition, the subsequent effects of displacements in the crystalline lattice and the accumulation of charges at interfaces (TID) will be analyzed. Subsequently, from the experiment, it is intended to extend the analysis with simulation, to estimate noise and flaws in generated images.

Desenvolvimento de um Sensor Compacto para Contagens de Prótons, Elétrons e Raios Gamma em Baixa Órbita Terrestre

Mauro A. Alves e Inácio M. Martin

ITA - Divisão de Ciências Fundamentais - Departamento de Física

Our research group, together with UFSM engineers, is developing a compact sensor that will be taken on board the cubesat ITASAT-2. This sensor will perform measurements in low Earth orbit of protons, electrons and gamma rays. The functioning of the sensor is based on scintillators (organic and inorganic) and on the recording of event counts. The use of facilities at USP's Institute of Physics and Pelletron is justified by the need to obtain pulses produced by the interaction of protons with organic scintillators for sensor calibration. For the ITASAT-2 mission, we are developing a sensor (named PEGASUS, Particle and GAmma Ray Sensor Using Scintillators) with construction based on a phoswich detector, combining organic and inorganic scintillators

The objective of the experiment is the characterization and calibration of PEGASUS. We would like to subject the sensor to different flows and energies to determine its ability to separate pulses (mainly in situations of intense flows) and to characterize the energy of the observed pulses. The main experiment will consist of PEGASUS irradiation with beams of protons with variable fluxes and energies from 1 protons/cm²/s to fluxes of the order of 10^5 protons/cm²/s. If possible, it would be interesting to irradiate with energies ranging from 8 to 15 MeV, with energies varying at intervals of 1 MeV. If possible, and time permitting, it would also be interesting to irradiate the sensor with the 5 MeV alpha source.

Characterization of the COTS RF Devices of a Robust and Versatile UHF TT&C Transceiver for National Cubesats

Lucas Compassi Severo - Federal University of Pampa (coordinator)

This research project aims to develop an RF transceiver module operating in the UHF band to operate as a Telemetry, Tracking, and Command (TT&C) to be employed in future national cubesats. This transceiver will be developed using COTS (Commercial off-the-shelf) radio frequency (RF) devices employing redundancy, error correction codes and advanced digital processing to become robust to ionizing radiation, temperature and process variations. Its application will be flexible, since the data format will follow the standards defined by the CCSDS (Consultative Committee for Space Data Systems).

The main motivation of this proposal is to provide radiation testing (TID and SEE) of the electronic components used in the RF circuit implementations. Below there is a list of the main integrated circuits that will be used and radiation testing will be performed:

- RF Transceiver: Silicon Labs Si4463
- Low Noise Amplifier (LNA): Qorvo QPL9547
- Power Amplifier (PA): Qorvo TQP3M9009

Development of new devices (HEPIC) for CERN

M. Munhoz and M. Bregnant (DFN – IFUSP)

The High Energy Physics and Instrumentation Center (HEPIC) from the Nuclear Physics Department and the Laboratório de Sistemas Integráveis (LSI) from Escola Politécnica da USP have the entire responsibility of the design, simulation, prototyping, experimental testing, validation and manufacturing of this new ASIC that will work in the new conditions imposed by the LHC. In particular, the group was responsable for the development of the Sampa chip, a special device) that will be installed in the front-end electronics of detectors with the aim of amplifying, converting and filtering the signal generated by these devices. One of the main requirements of this new ASIC is to cope with the radiation induced by LHC in the ALICE environment. Therefore, it is mandatory to perform several tests with this device in order to qualify it for usage under such environment. In the context of the development of new ASICs, in 65nm technology, we plan to perform SEE (Single Event Effect, mainly SEU) tests for a PLL prototype and an ADC prototype. In the case of the PLL we can also consider the TID measure.