LABORATÓRIO ABERTO DE FÍSICA NUCLEAR
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Proposal	N°
Title: The worst-case response of ion-induced destructive radiation effects in advanced transistors	
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Number of days for experiment:	10
Period planned for the experiment (are the setup ready for beam time?): After September 2023	

Technical information

Ion source			Accelerator			Experimental Area	
Beam	Cathode	$I_{mínima}$	V_{min}	V_{max}	Bunched beam?	Beam line	Target
^{28}Si	21 or 27	200 nA	7.0	8.0	no	0º	Si-based transistors
^{35}Cl	21 or 27	200 nA	7.0	8.0	no	0º	Si-based transistors
^{48}Ti	21 or 27	200 nA	7.0	8.0	no	0º	Si-based transistors
^{63}Cu	21 or 27	200 nA	7.0	8.0	no	0º	Si-based transistors

Other relevant/needed information: Cathode numbers extracted from ‘Relação de catodos montados na fonte MC-SNICS 16/10/2018’, by J. C. Abreu

The worst-case response of ion-induced destructive radiation effects in advanced transistors

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Abstract

Electronic devices that operate in radiation environments are subject to suffer from radiation damage that can lead to malfunctions, errors, and even complete destruction. Power Metal-Oxide-Semiconductor Field-Effects Transistors (MOSFETs) are widely used in electronic systems for space applications and, when operating in harsh radiation environments like outer space, they are susceptible to suffer destructive failure modes such as Single-Event Burnout (SEB) and Single-Event Rupture (SEGR). With recent technological advances, the power electronics industry aims to supplant the traditional vertical double-diffused MOSFET (DMOSFET) with the modern trench gate or U-groove MOSFET (UMOSFET) technology, but there are few or no detailed experimental results published in the literature comparing their radiation hardness response. Devices used in embedded space or avionics systems must be extensively tested under radiation before being used in such high-reliability applications. Irradiation tests are conducted in ground-level facilities, preferably with energetic ions provided by particle accelerators. Although some radiation test guidelines and protocols for the qualification of electronic devices exist, the qualification of power devices requires more sophisticated methods since the stopping power of energetic ions significantly varies in the thick sensitive layers of the device. The state-of-the-art prediction model for radiation effects qualification of DMOSFET was experimentally validated for the SEGR failure mode, but there is little evidence of its validity for the SEB destructive failure mode. Additionally, the accuracy of the state-of-the-art prediction model is not currently established and the fact that this prediction model is based in several simplified assumptions also imposes a necessity to improve its physical picture.

The present proposal aims to experimentally investigate the heavy-ion-induced destructive radiation effect response of similarly rated DMOS and UMOS power transistors. The first objective is to directly compare the susceptibility of these distinct transistor technologies in regards to the particle-induced SEB destructive failure mode. The second objective is to elucidate the worst-case response in Si-base devices, assessing the accuracy of the predictive models currently available from experimental data. As a result, we expect to consolidate a general protocol for irradiation tests in such semiconductor electronics devices by using particle accelerators. Based on experimental validation in Si-based transistors, the prediction model methodology can be applied and expanded to other advanced semiconductor materials such as SiC, GaN, and GaAs.

The worst-case response of ion-induced destructive radiation effects in advanced transistors

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I. SCIENTIFIC MOTIVATION / SCIENTIFIC BACKGROUND

Power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are susceptible to suffer destructive radiation effects like Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR) when operating in harsh radiation environments, such as outer space [1]. In order to evaluate the risk of such failure modes in these devices, radiation scientists and engineers have been testing them in ground-level facilities, preferably by using heavy ion beams provided by particle accelerators [2]. Notably, with the aim to improve the currently existing guidelines for radiation tests in power MOSFETs, Titus et al. introduced a methodology for predicting the critical heavy ion energy that is able to cause the SEE worst-case response in vertical double-diffused MOSFETs (DMOSFETs) [3]. Their predictive model was validated with some degree of accuracy for the SEGR worst-case response in DMOSFETs. Recently, Alberton et al. presented evidence that this methodology could also be useful for predicting the SEB worst-case response in DMOSFETs [4].

New FET technologies have emerged and there is an increasing interest in using commercial off-the-shelf (COTS) devices for applications that demand a high level of reliability, such as aerospace, avionics, and even some ground-based applications like autonomous driving systems. Recently, the traditional DMOSFET technology has been superseded by the modern trench gate or U-groove MOSFET (UMOSFET) [5]. In general, the UMOSFET technology has shown superior electrical performance in comparison to the DMOSFET technology, but several unique threats may arise when operating these devices in radiation environments. Due to its unique design architecture, UMOSFETs experience higher local electric fields compared to similarly rated DMOSFET [6], which can contribute to the occurrence of destructive failure modes such as SEBs. Nevertheless, the ion-induced charge collection mechanisms in UMOSFETs are not well understood at the present time. In addition, no detailed experimental comparison of radiation effect response between similarly rated UMOS and DMOS devices has been published in the open literature [5].

This work aims to experimentally investigate the heavy ion-induced destructive radiation effects in similarly rated DMOS and UMOS power transistors. The first objective is to compare the susceptibility of these distinct transistor technologies to the particle-induced SEB destructive failure mode. Secondly, from experimental data, the accuracy of the predictive models for the worst-case response currently available will be assessed.

II. PROPOSED EXPERIMENT(S)

According to the predictive model of Titus *et al.*, the critical ion energy that should produce the worst-case response in DMOSFETs is given by [3]:

$$E_{crit}\ [\mathrm{MeV}] = \left[\frac{Z^{1.333}\cdot BV_{DS}}{176} + \frac{382\cdot Z}{112 - Z}\right]\sqrt{\frac{V_{DS}}{BV_{DS}}} \qquad (1)$$

in which Z is the ion atomic number, and BV_{DS} and V_{DS} are the breakdown and applied drain-source voltage, respectively, in units of volts. It should be pointed out that the model of Titus *et al.* is unidimensional, built by considering a generic and simplified device geometry, and also neglects the charge collection contribution via the diffusion mechanism. In order to circumvent these limitations, after extracting typical dimension parameters of several commercially available UMOSFETs and implementing a diffusion model in the previously established charge collection model for Si-based transistors, we propose an original expression for worst-case response prediction in UMOSFETs [7]:

$$E_{crit}\ [\mathrm{MeV}] = \frac{\mathrm{Z}^{1.45}}{223} \cdot BV_{DS} + 3.6 \times 10^{3} \cdot \exp\left[-\frac{140}{Z+17}\right] \quad (2)$$

Under the assumptions of the proposed model for UMOSFETs, the average uncertainty of (2) is estimated to be about 30% in the range $15 < Z < 80$ and $50\ \mathrm{V} < BV_{DS} < 300\ \mathrm{V}$, that is usually the region of main interest for destructive radiation effect investigations in Si-based power FETs by using particle accelerators.

The goal of this experiment is to assess the susceptibility of traditional and advanced power transistors to ion-induced destructive failure modes, and compare the model predictions (1) and (2) with experimental data. The experiment proposed basically consists in exposing similarly voltage-rated UMOS and DMOS to monoenergetic heavy-ion beams on the frontside irradiation and measure the ion-induced SEB cross section as a function of the beam energy for distinct ion species. The SEB worst-case response of the devices under test (DUTs) will be investigated for four ion species, namely ^{28}Si, ^{35}Cl, ^{48}Ti, and ^{63}Cu (see Table 1). The measurements at energies higher than that available at the São Paulo Pelletron accelerator are going to be conducted at the INFN-LNL Tandem facility, Italy.

Table 1. Experiment time schedule.

^{28}Si			
E [MeV]	Z^*	V_T [MV]	Facility
42	5	7.0	USP, Brazil
49	6	7.0	
56	7	7.0	
63	8	7.0	
72	8	8.0	
^{35}Cl			
E [MeV]	Z^*	V_T [MV]	Facility
42	5	7.0	USP, Brazil
49	6	7.0	
56	7	7.0	
63	8	7.0	
72	8	8.0	
80	9	8.0	
^{48}Ti			
E [MeV]	Z^*	V_T [MV]	Facility
49	6	7.0	USP, Brazil
70	9	7.0	
88	10	8.0	
96	11	8.0	
^{63}Cu			
E [MeV]	Z^*	V_T [MV]	Facility
49	6	7.0	USP, Brazil
88	10	8.0	

* Variations within a few MeVs in the proposed energy range are perfectly aceptable since the main objective is to cover a wide range of energies.

III. BEAMLINE(S) AND BEAM TIME REQUESTED

Experimental tests are going to be carried out at the SAFIIRA beamline [2]. In total, 10 days of beam time at the São Paulo Pelletron accelerator is requested.

IV. A BRIEF REPORT FROM PREVIOUS MEASUREMENTS

Titus et al. experimentally demonstrated that the SEGR response of power DMOSFETs depends on the ion species and its energy [3]. At that time, these authors claimed that the dependence of the SEB response on the ion energy had not been adequately studied. In 2011, Liu et al. showed that the SEB

failure voltages have a strong correlation with the ion species and the charge deposited within the epitaxial region of DMOSFETs [8]. In 2022, by using heavy ion beams, Alberton et al. presented experimental evidence that the deposited charge within the depletion region is the proper metric for the description of SEB triggering and also that the methodology of Titus et al. based on charge deposition is relevant for failure prediction in the SEB mechanism in DMOSFETs [4]. Nevertheless, the accuracy of the prediction model proposed by Titus et al. is not currently established.

V. EXPERIMENTAL TECHNIQUE(S), REQUIRED SET-UP(S), MEASUREMENT STRATEGY, SAMPLE DETAILS (QUANTITY...ETC)

Although SEBs are intrinsically destructive failure modes, the current limiting technique is a widely used protective test method that enables us to assess the ion-induced SEB cross section in power devices [9]. Figure 1 shows the proposed circuitry that will be used for protective SEB tests of 04 DUTs simultaneously. For each ion/energy condition, the DUTs with similarly rated breakdown voltages, ranging from 40 V up to 150 V (Table 2), will be irradiated in the OFF mode (V_{GS} = 0 V and V_{DS} > 0), being supplied by a high-voltage SMU. The SEB signals will be indirectly detected by using protective circuitry based on the current limiting technique and recorded with a high-bandwidth oscilloscope. For each run (ion species/energy/applied voltage condition), the DUT is going to be irradiated up to a beam fluence of $\Phi = 10^6$ ions/cm^2. Finally, the SEB cross section is obtained by dividing the number of detected SEBs by the beam fluence of the run.

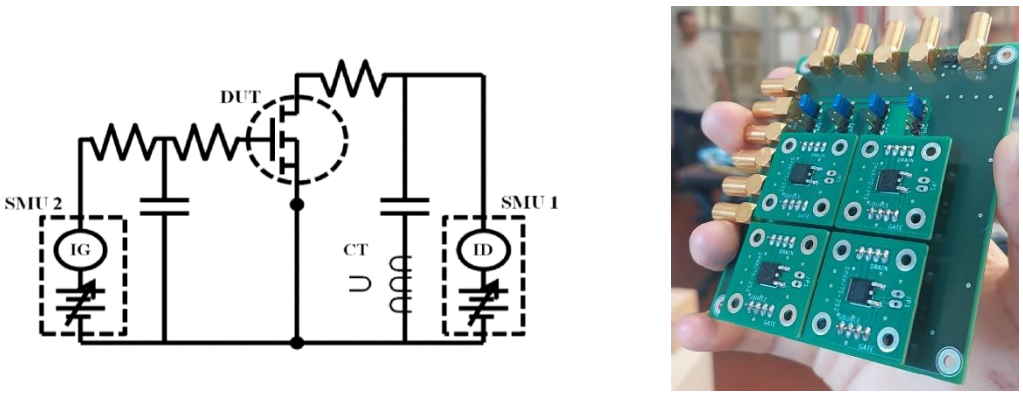

Figure 1. Basic test circuitry for protective ion-induced SEB measurements in power devices.

Table 2. Relevant information details of the devices under test.

DUTs part name	Technology	BV_{rated} [V]	Qty.
IRFR7440TRPBF	DMOSFET	40	1
IRLZ24PBF		60	1
IRFR3410TRPBF		100	1
IRFS52N15DTRLP		150	1

DUTs part name	Technology	BV_{rated} [V]	Qty.
SI4840BDY-T1-GE3	UMOSFET	40	1
SiR514DP-T1-RE3		60	1
SiR876BDP-T1-RE3		100	1
SI4848DY-T1-GE3		150	1

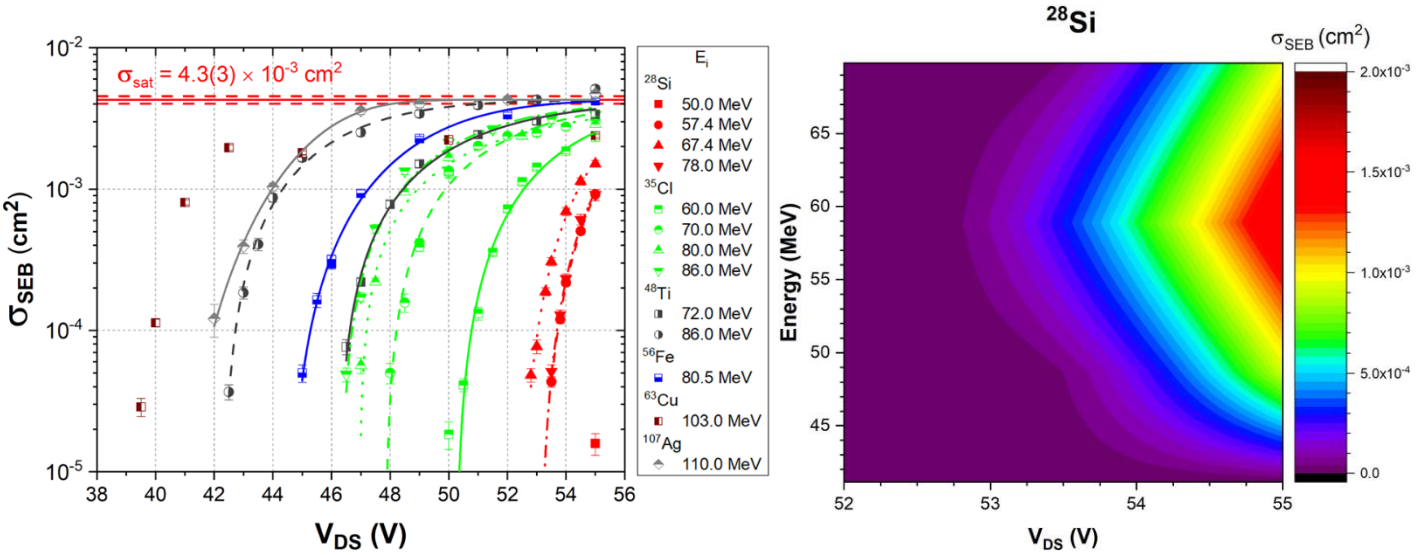

Figure 2. Example of SEB cross section measurements previously carried out by the proponents of this proposal in a low-voltage DMOSFET. From [4].

VI. RESULTS EXPECTED AND THEIR SIGNIFICANCE IN THE RESPECTIVE FIELD OF RESEARCH

Figure 2 presents SEB cross section curves as a function of V_{DS} for several ion species and beam energies. These experimental results were obtained by the proponents of this proposal in previous experiment at the São Paulo Pelletron 8-UD accelerator facility [4].

The expansion of UMOSFET technology in the power electronics market will bring an increase in its usage for general-purpose applications. In addition, with the growing interest in using COTS devices for high-reliability applications, one may also expect to see the UMOSFET technology incorporated into next-generation electronics systems for usage in various environments, such as at flight altitudes, ground level, and possibly in space. From a direct comparison between the ion-induced SEB response of UMOS and DMOS technologies, one can access the feasibility and risks of using the emerging UMOSFET technology in applications that demand high levels of reliability when operating in harsh radiation environments.

Whether the models are validated from experimental results, one can support the physical basis of new test methodologies for the qualification of power transistors operating in harsh radiation environments. By establishing the accuracy of the prediction models for the ion-induced SEE worst-case response currently available, one can consolidate a general protocol for irradiation tests in semiconductor electronic devices by using particle accelerators. As a result, it is expected that the international community will update its testing guidelines and method standards accordingly. Based on experimental validation in Si-based transistors, the prediction model methodology can be applied and expanded to other advanced semiconductor materials such as SiC, GaN, and GaAs.

References

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